THAT WHICH IS CLAIMED IS:

1. A dynamically reconfigurable processing unit including an embedded Flash memory device for non-volatile storage of code, data and bit-streams, the unit being integrated into a single chip together with a microprocessor core, further comprising an S-RAM based embedded FPGA unit structured for FPGA reconfigurations having a specific programming interface connected to a port of said Flash memory device through a DMA channel.

2. A dynamically reconfigurable processing unit according to claim 1, wherein said DMA channel handles the bitstream transfer while said microprocessor fetches instructions and data from different Flash memory ports of said Flash memory device; a wide code port and a data port.

3. A dynamically reconfigurable processing unit according to claim 2, wherein said Flash memory device includes a modular array structure comprising N memory blocks, and wherein a power block, including charge pumps, is shared among different flash memory modules through a PMA arbiter in a multi-bank fashion.

4. A dynamically reconfigurable processing unit according to claim 1, wherein said embedded FPGA unit exploits the following functions:

i) extension of the processor datapath supporting a set of additional special-purpose C-callable microprocessor instructions;

ii) bus-mapped coprocessors, connected to the system bus through a master/slave interface;

iii) flexible I/O to connect external units or sensors with application-specific communication protocols.

5. A dynamically reconfigurable processing unit according to claim 2, wherein said Flash memory device includes at least three different access ports, each for a specific function:

- said code port optimized for random access time and the application system;
- said data port allowing an easy way to access and modify application data; and,
- said FPGA port offering a serial access for a fast download of bit streams for an embedded FPGA configurations.

6. A dynamically reconfigurable processing unit according to claim 2, wherein said third port comprises four configuration registers replicating the information stored in said code port that must be used in order to write e-FPGA configurations data.

7. A dynamically reconfigurable processing unit according to claim 5, wherein said third port uses a chip select to access in the addressable memory space and a burst enable to allow burst serial access.

8. A dynamically reconfigurable processing unit according to claim 1, wherein said connection

between said interface and said port is provided by a local bus.

9. A dynamically reconfigurable processing unit according to claim 5, wherein said Flash memory device includes four modules each arranged in at least three programmable user-defined partitions, each one devoted to a corresponding port.